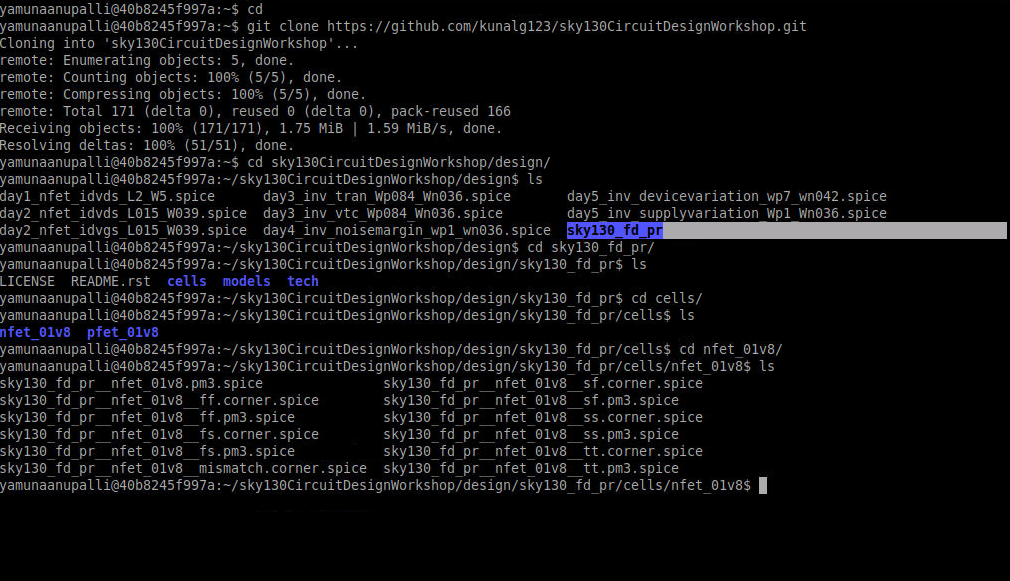
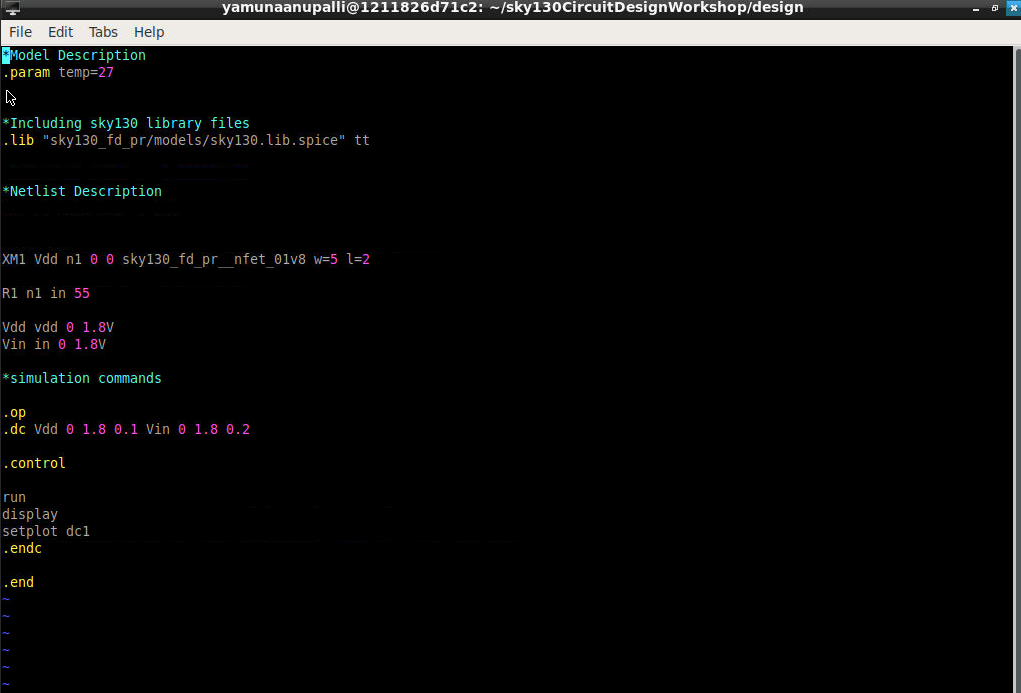
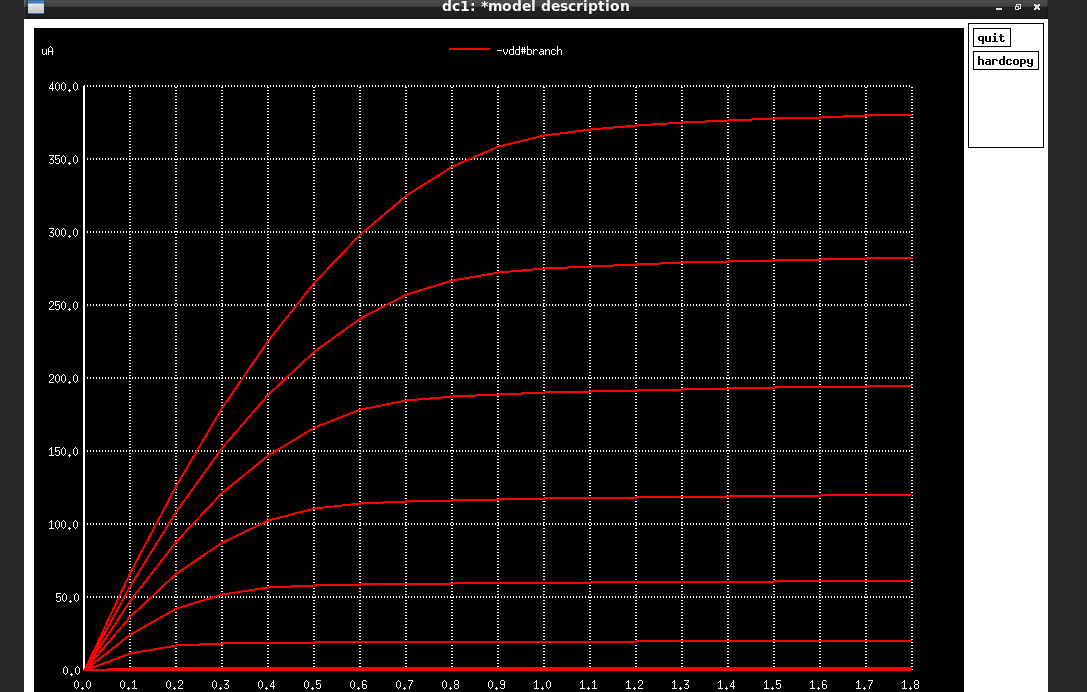
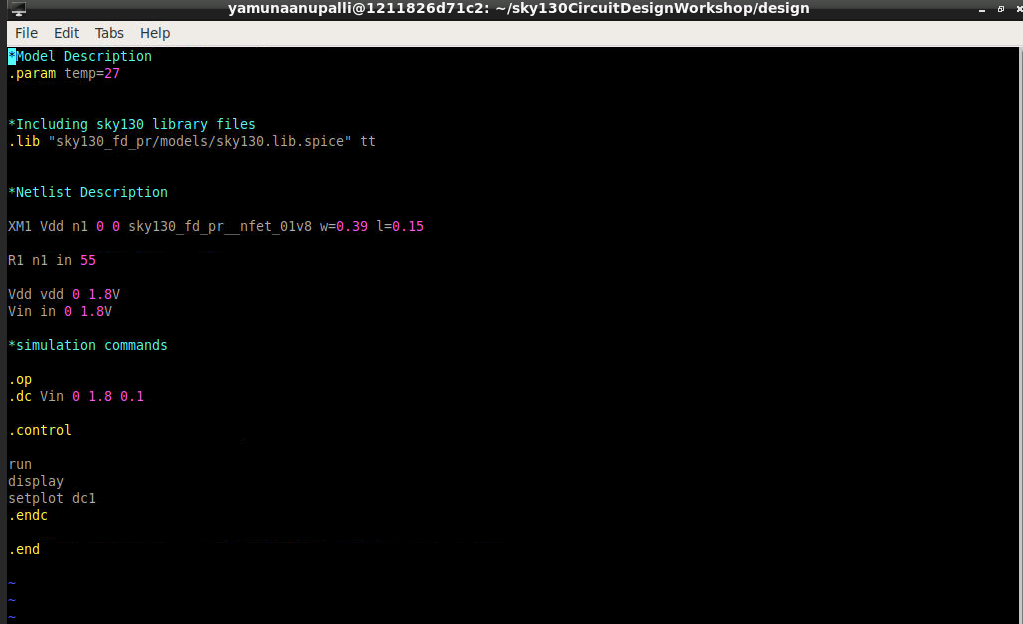
VSD- IAT Workshop





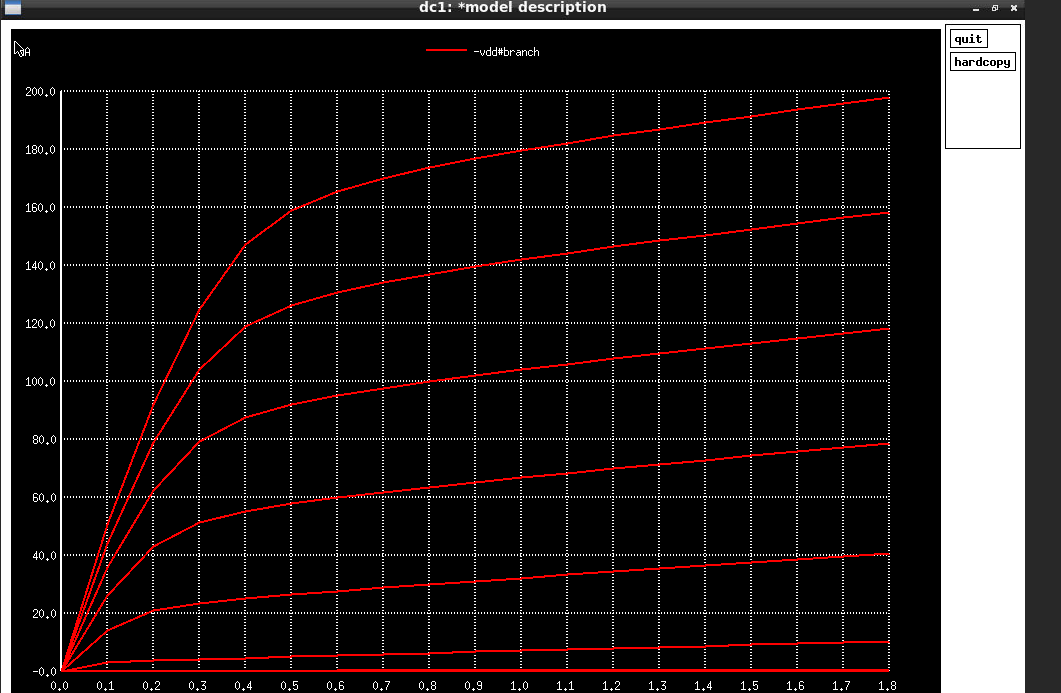


Day 2 labs

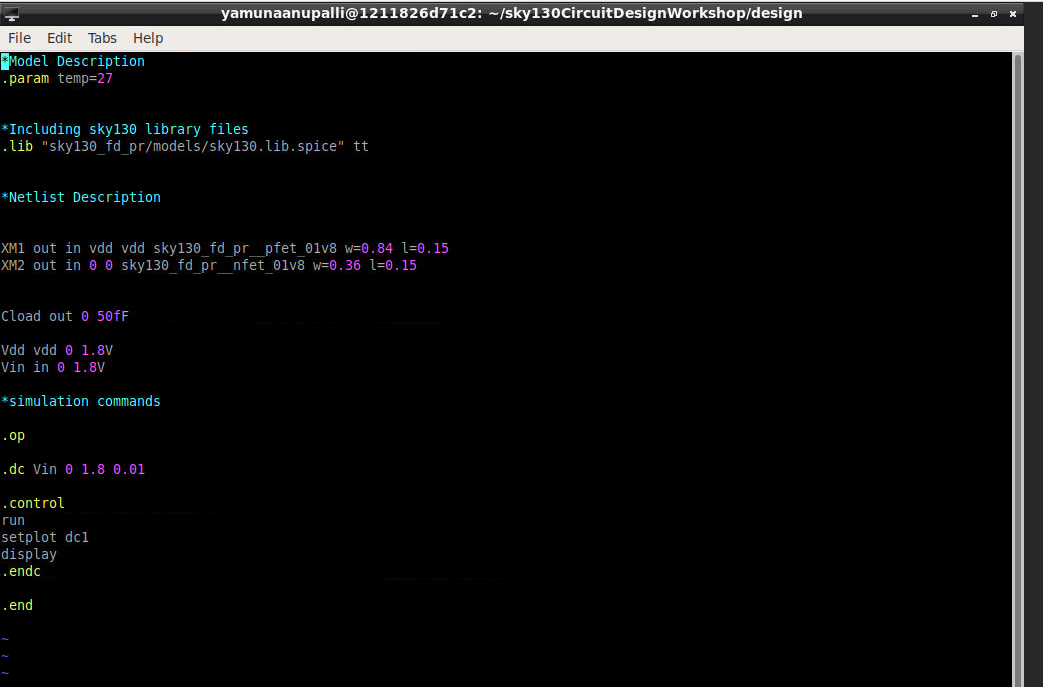




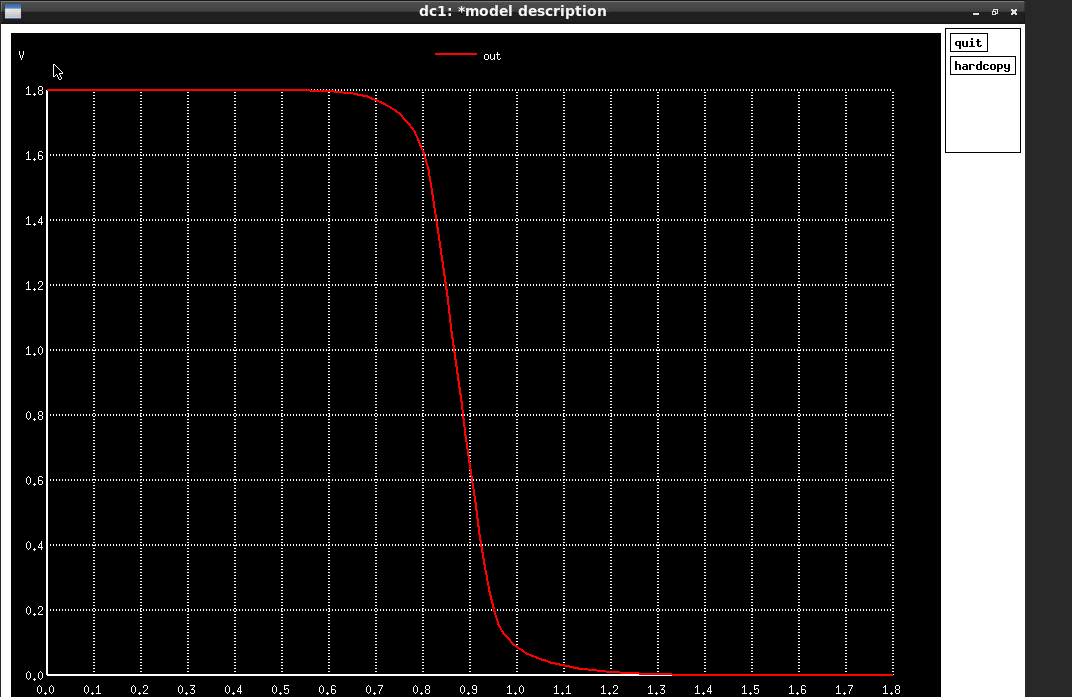




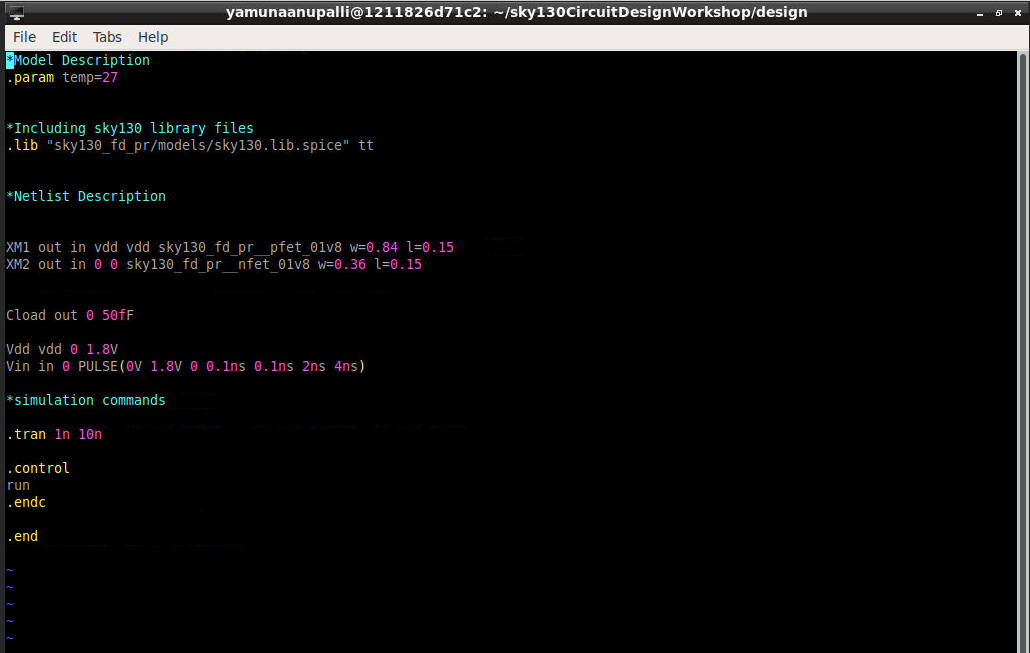
Day 3 labs

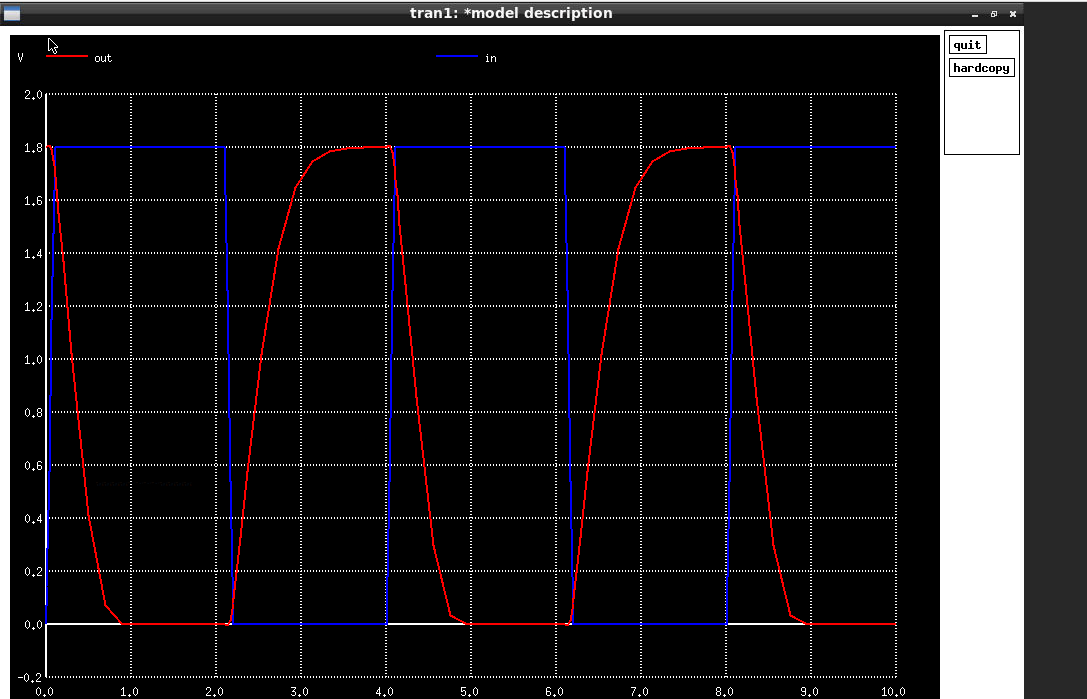


Plot out vs in

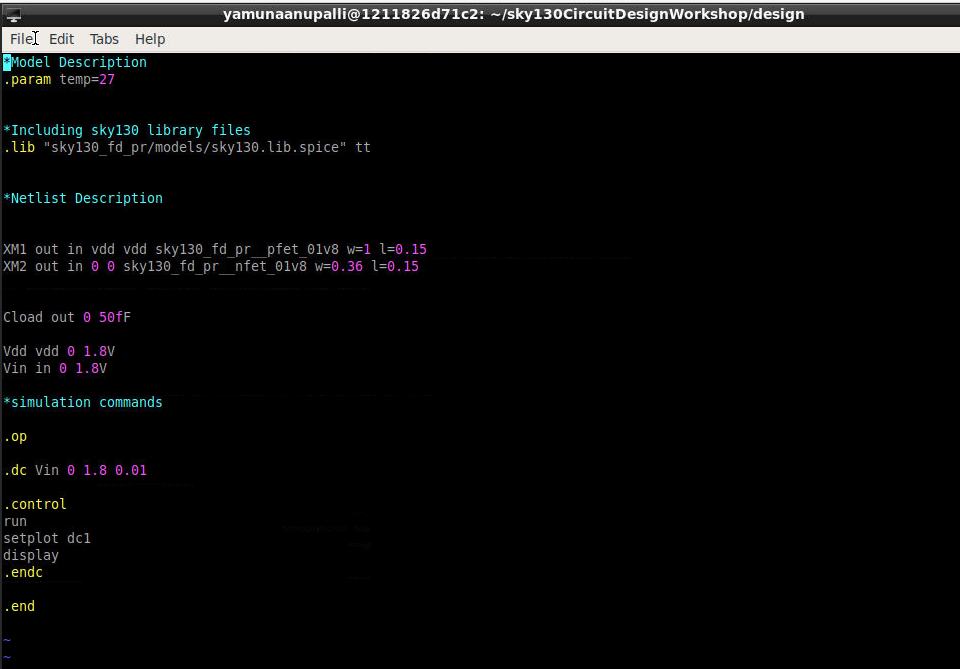


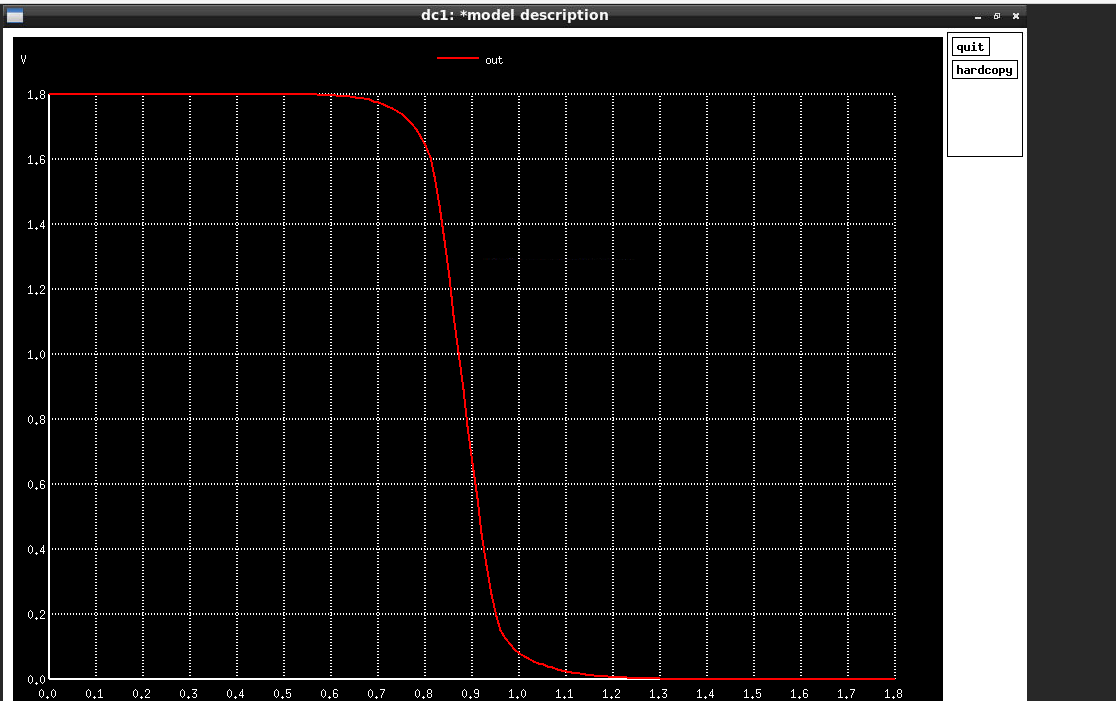
Transient analysis---plot out vs time vs in



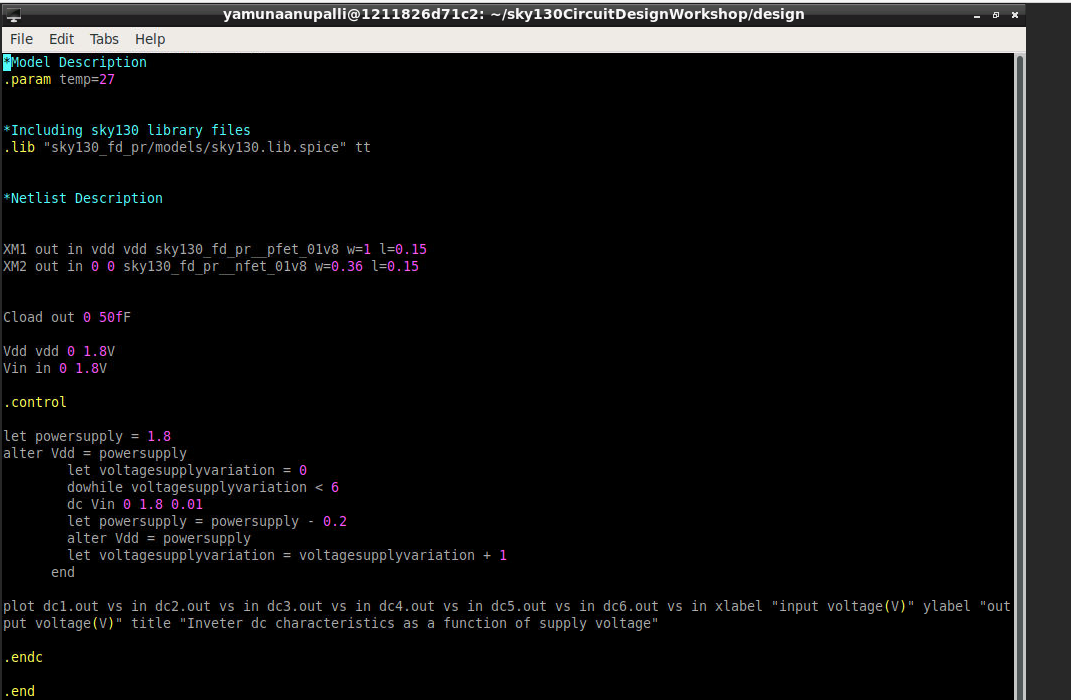


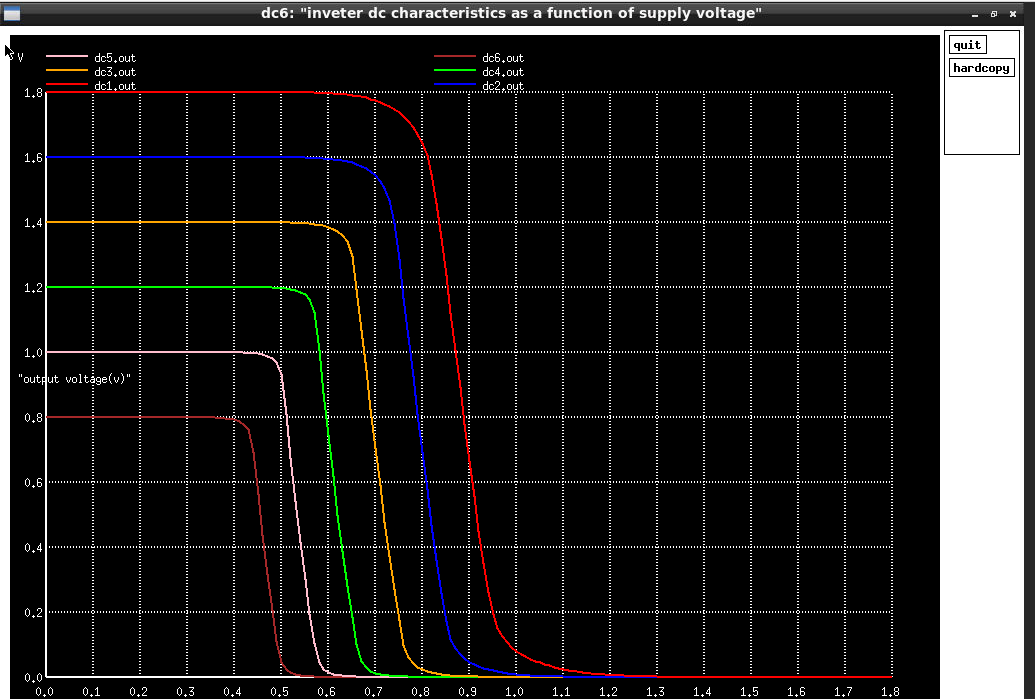
Noise margin Lab 4





To calculate the supply variation lab 5

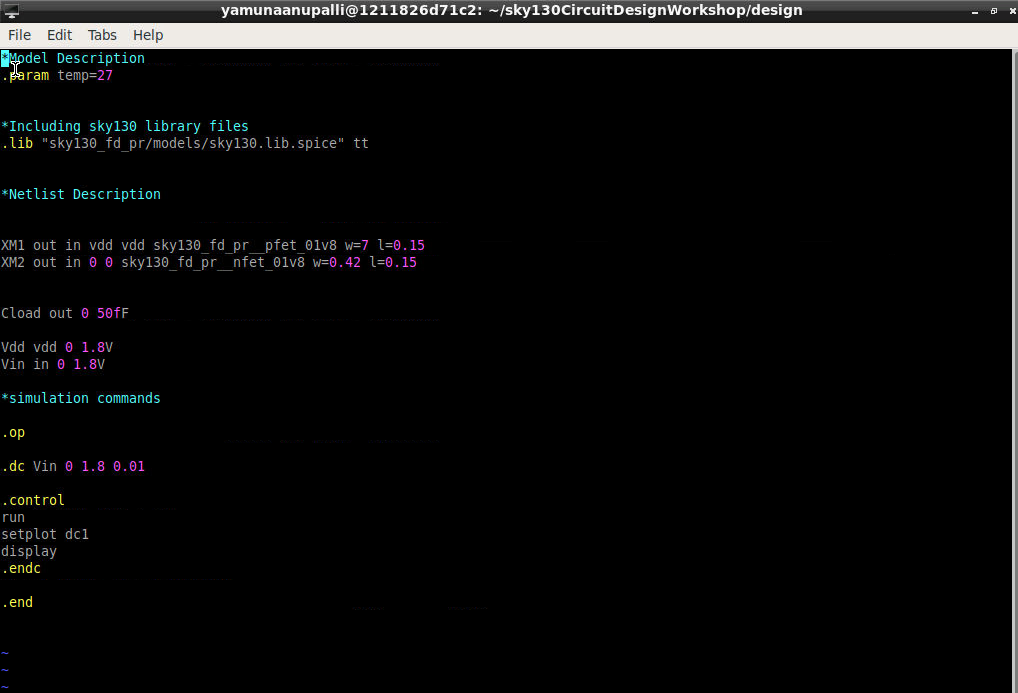


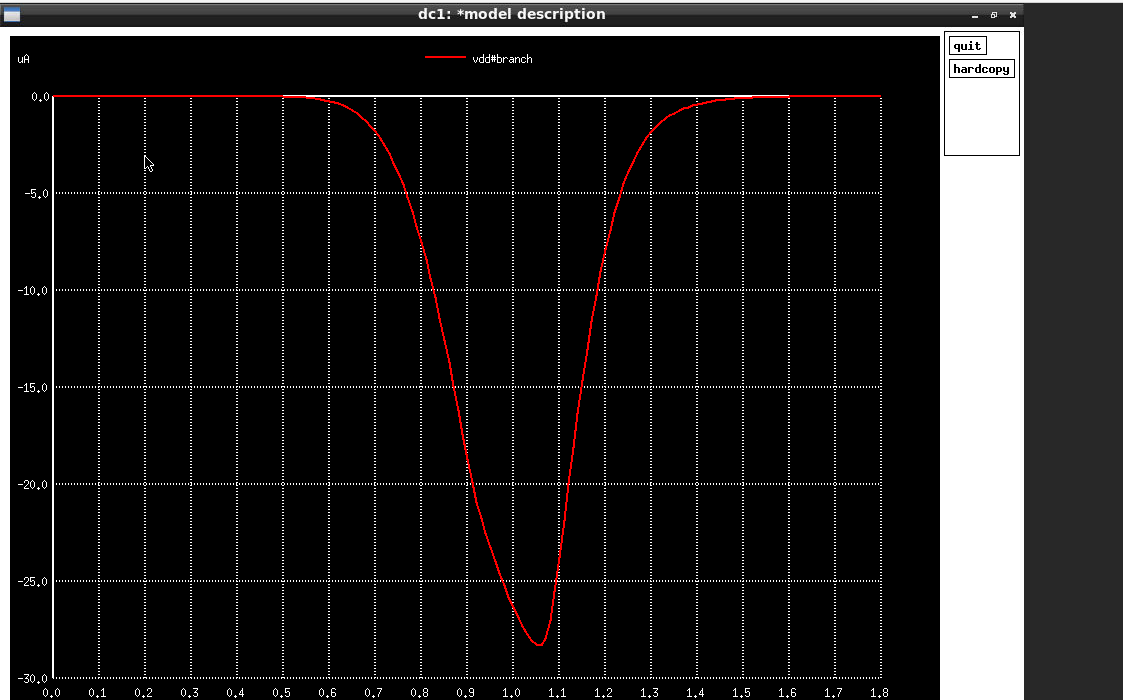


As supply voltage reduces gain increases until 1v

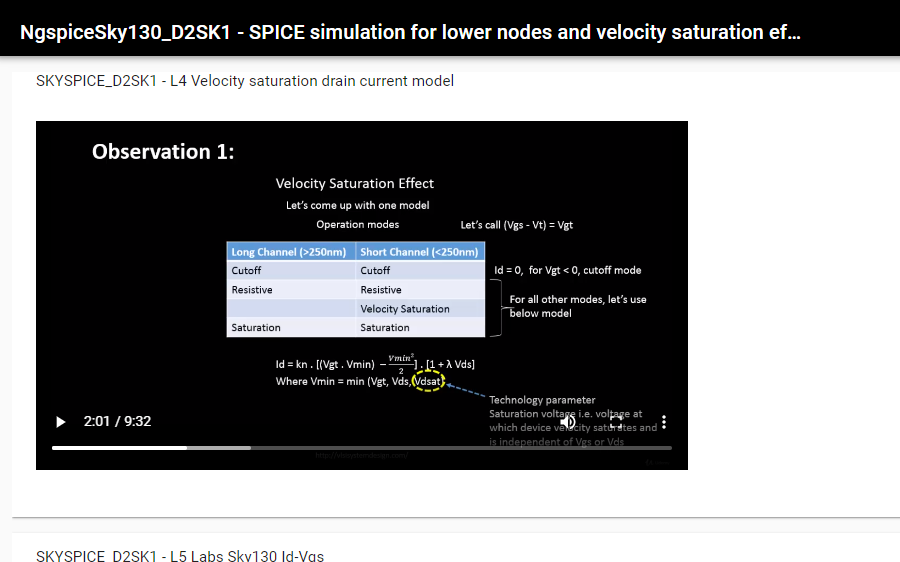
But for 1v and 0.28v gain reduces because the voltage is not enough for the nfet and pfet to turn on so not enough gain

Device variation:



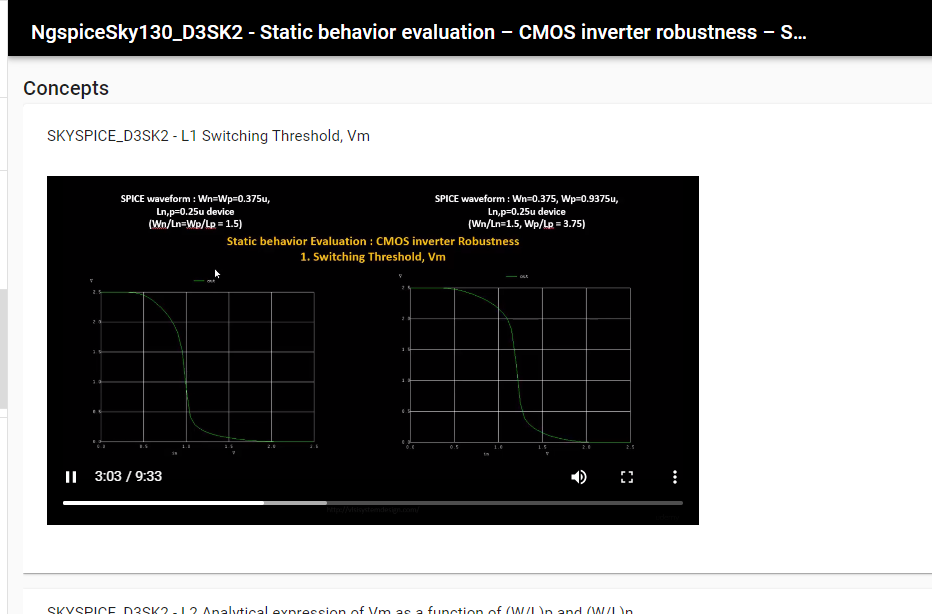


Notes:

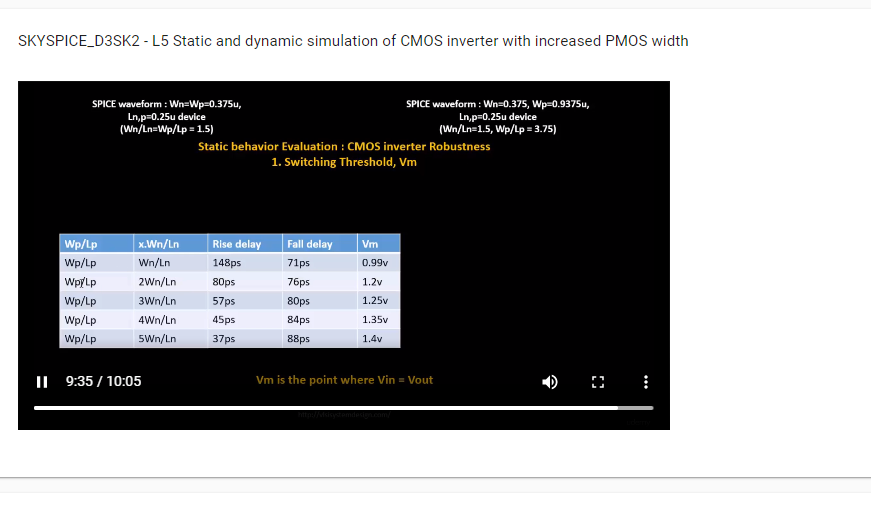


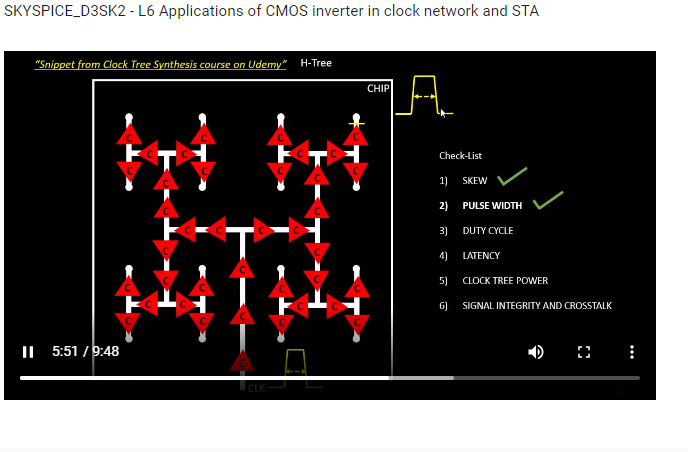
To prove the robustness of the cmos---based on switching threshold- where vin=vout

And in the transient sim we find the rise and fall delay variation with variation in switching threshold(indirectly with size of pmos)



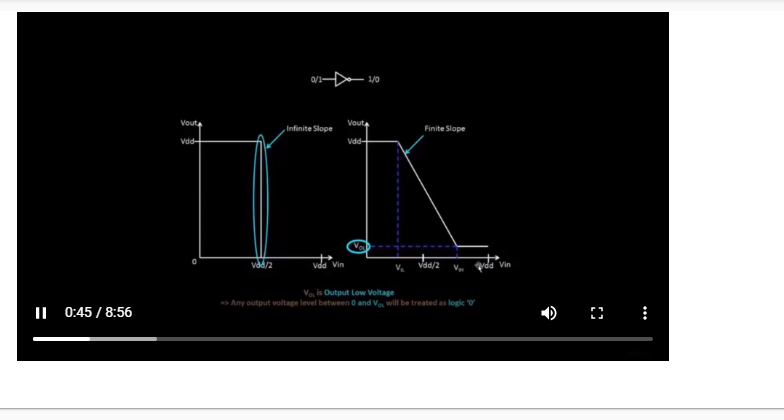
Rise and fall delayss





Any voltage wil be 0 and ViL- 0 for output to is Voh if inpuut is in between 0 and Vil.

Noise margin voltage parameters



In Static Timing Analysis, clock buffers are buffers with symmetric rise and fall delays unlike the normal buffers used in datapath or any other part of the logic.

CMOS logic robustness- based on threshold point and estimating noise margins to consider inputs properly even with noise.

As the size of NMOS is increased keeping pmos size constant-

1. Fall delay reduces
2. Rise delay increases
3. Threshold point moves to left that is less Vin voltage is used by cmos logic to reach 0.5v

As the size of the PMOS is increased keeping nmos size constant-

1. Rise delay reduces
2. Fall delay increases
3. Threshold point moves to right that is more Vin voltage is used by cmos logic to reach 0.5v